We Claim:

1. A memory module for a memory configuration having a bus system with a plurality of signal lines for transmitting data signals, the memory module comprising:

a substrate;

connection elements supported by said substrate;

a plurality of memory chips disposed on said substrate and connected to the signal lines through said connection elements; and

contact devices, including supplying contact devices and discharging contact devices, each of the signal lines being connected to a respective one of said supplying contact devices and a respective one of said discharging contact devices, said respective supplying and discharging contact devices associated with one another being disposed physically close together.

2. The memory module according to claim 1, wherein said contact devices have at least three associated said memory chips, each of said discharging contact devices is disposed at a shorter distance from an associated said respective supplying contact device than, on average, said connection

elements associated with the signal line on said memory chips associated with the signal line.

3. The memory module according to claim 1, wherein said contact devices are associated with precisely one of said memory chips, and said respective supplying contact device and an associated said respective discharging contact device have a maximum of sixteen different one of said contact devices disposed between them.

4. The memory module according to claim 1, wherein each respective one of the signal lines is routed essentially without any stub continuously and on a direct path from said respective supplying contact device in succession via said connection elements associated with the respective signal line on said memory chips associated with the respective line to said respective discharging contact device.

5. The memory module according to claim 1, wherein said contact devices are disposed in at least one contact row, and in said contact row there is a maximum of two further ones of said contact devices provided between each said respective supplying contact device and an associated said respective discharging contact device.

6. The memory module according to claim 1, wherein said contact devices are disposed in at least two contact rows which are disposed one of directly opposite one another and offset from one another on said substrate, and each of said supplying contact devices is disposed opposite an associated said respective discharging contact device directly or with an offset.

7. The memory module according to claim 1, wherein:

said memory chips have a chip package with a given length and a given width; and

said connection elements associated with a respective signal line are connected to the respective signal line at a respective distance which is obtained from said given length or from said given width of said chip package for said memory chips.

8. The memory module according to claim 1, wherein said connection elements associated with a respective one of the signal lines are connected to the respective signal line substantially at equivalent distances.

9. The memory module according to claim 1, wherein said memory chips each have a double data rate interface.

10. The memory module according to claim 1, wherein the memory module holds up to 32 of said memory chips for a memory system without error correction devices which contains the memory configuration.

11. The memory module according to claim 1, wherein the memory module holds up to 36 of said memory chips for a memory system with error correction devices which contains the memory configuration.

12. The memory module according to claim 1, wherein said substrate has at least two substrate sections which are mechanically and electrically connected to one another.

13. The memory module according to claim 12, wherein said substrate sections are disposed at a distance of between 5 and 25 mm, respectively, and are oriented parallel to one another.

14. The memory module according to claim 1, wherein said substrate is a rectangular printed circuit board, and said memory chips are disposed in at least two rows in a respective parallel orientation on two opposing surfaces of said rectangular printed circuit board.

15. The memory module according to claim 14, wherein said rectangular printed circuit board has dimensions 1.7 to 3.0 inches x 5.25 inches.

16. The memory module according to claim 1, wherein said contact devices are associated with precisely two of said memory chips, and each of said supplying contact devices and an associated said respective discharging contact device have a maximum of sixteen different ones of said contact devices disposed between them.

17. The memory module according to claim 1, wherein said contact devices have at least three associated ones of said memory chips, each of said discharging contact devices is respectively disposed at a shorter distance from an associated said respective supplying contact device than, an average distance between said memory chips.

18. A memory configuration for a memory system, the memory configuration comprising:

a system board;

a bus system having a plurality of signal lines for transmitting data signals and supported by said system board;

holding devices disposed on said system board;

a bus control chip connected to said holding devices; and

memory modules disposed and held by said holding devices, each of said memory modules including:

a substrate;

connection elements supported by said substrate;

a plurality of memory chips disposed on said substrate and connected to said signal lines through said connection elements; and

contact devices, including supplying contact devices and discharging contact devices, each of said signal lines connected to a respective one of said supplying contact devices and a respective one of said discharging contact devices, said respective supplying contact device and said respective discharging contact device associated with one another being disposed physically close together.

19. The memory configuration according to claim 18, wherein

said holding devices are precisely four holding devices configured as plug-in sockets.

20. The memory configuration according to claim 18, wherein said bus system contains a multiple X of a number Y of said signal lines assigned for each of said memory modules, each of said memory modules is associated with one of X memory module groups, and each of said signal lines is respectively associated with said memory modules in one of said X memory module groups.

21. A memory module for a memory configuration having a bus system with a plurality of signal lines for transmitting data signals, the memory module comprising:

a substrate;

connection elements supported by said substrate;

a plurality of memory chips disposed on said substrate and connected to the signal lines through said connection elements; and

contact devices, including supplying contact devices and discharging contact devices, each of the signal lines connected to a respective one of said supplying contact

devices and a respective one of said discharging contact devices, each respective one of the signal lines being routed substantially without any stub continuously and on a direct path from said respective supplying contact device in succession through said connection elements associated with the respective signal line on said memory chips associated with the respective signal line to said respective discharging contact device, and said contact devices disposed in at least one contact row and, in said contact row, said respective supplying contact device and an associated said respective discharging contact device have a maximum of two further ones of said contact devices provided between them.

22. The memory module according to claim 21, wherein no further ones of said contact devices are disposed between said respective supplying contact device and said respective discharging contact device.

23. A memory module for a memory configuration having a bus system with a plurality of signal lines for transmitting data signals, the memory module comprising:

a substrate;

connection elements supported by said substrate;

a plurality of memory chips disposed on said substrate and connected to the signal lines through said connection elements; and

contact devices, including supplying contact devices and discharging contact devices, each of the signal lines connected to a respective one of said supplying contact devices and a respective one of said discharging contact devices, each respective one of the signal lines being routed substantially without any stub continuously and on a direct path from said respective supplying contact device in succession through said connection elements associated with the respective signal line on said memory chips associated with the respective signal line to said respective discharging contact device, and said contact devices being disposed in two contact rows disposed opposite one another on said substrate directly or with an offset, and each of said supplying contact devices being disposed opposite an associated said respective discharging contact device directly or with an offset.